L Number	Hits	Search Text	DB	Time stamp
1	11192	CMOS and layout	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 08:57
2	737	unit adj wiring	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 08:58
3	6	(CMOS and layout) and (unit adj wiring)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 09:00
4	15	(CMOS and layout) and symetrical	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 09:15
5	236	257/69.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 09:16
6	43	(CMOS and layout) and 257/69.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 09:38
7	21268	PMOS and NMOS	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 09:38
8	3790	(PMOS and NMOS) and layout	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 09:39
9	2	((PMOS and NMOS) and layout) and (unit adj wiring)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 09:45
10	826	((PMOS and NMOS) and layout) and optimi$7	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 09:50
11	590	(((PMOS and NMOS) and layout) and optimi$7) and region	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 09:52
12	1351406	"12" and metal	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 09:52

13	444	((((PMOS and NMOS) and layout) and optimi$7) and region) and metal	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 09:53
14	375	(((((PMOS and NMOS) and layout) and optimi$7) and region) and metal) and logic	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 09:54
15	12	((((((PMOS and NMOS) and layout) and optimi$7) and region) and metal) and logic) and symetrical	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 09:55
16	371	((((((PMOS and NMOS) and layout) and optimi$7) and region) and metal) and logic) and well	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 09:57
17	186	(((((((PMOS and NMOS) and layout) and optimi$7) and region) and metal) and logic) and well) and die	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 11:46
18	11	"5146117"	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2003/03/13 11:46

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File View Edit Tools Window Help

- Active
  - L1: (11192) CMOS and layout
  - L2: (737) unit adj wiring
  - L3: (6) 1 and 2
  - L4: (15) 1 and symetrical
  - L5: (236) 257/69.ccls.
  - L6: (43) 1 and 5
  - L7: (21268) PMOS and NMOS
  - L8: (3790) 7 and layout
  - L9: (2) 8 and 2
  - L10: (826) 8 and optimi$7
  - L11: (590) 10 and region

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Default operator: OR | Highlight all hit terms initially

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BRS form | IS&R form | Image | Text | HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	☐	☐	US 6294816 B1	20010925	10	Secure integrated circuit	257/368	257/369; 257/659;
2	☑	☐	US 6255908 B1	20010703	18	Temperature compensated and digitally controlled amplitude and pha	330/149	330/145
3	☐	☐	US 6173436 B1	20010109	10	Standard cell power-on-reset circuit	716/19	716/1; 716/11
4	☐	☐	US 6064110 A	20000516	12	Digital circuit with transistor geometry and channel stops providing camoufl	257/652	257/204; 257/376;
5	☐	☐	US 5973375 A	19991026	16	Camouflaged circuit structure with step implants	257/399	257/648; 257/E27.009;
6	☐	☐	US 5930663 A	19990727	12	Digital circuit with transistor geometry and channel stops providing camoufl	438/598	257/390; 257/E27.009;
7	☐	☐	US 5866933 A	19990202	10	Integrated circuit security system and method with implanted interconnectio	257/368	257/369; 257/659;

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L9: (2) 8 and 2
L10: (826) 8 and optimi$7
L11: (590) 10 and region
L12: (1351406) "12" and metal
L13: (444) 11 and metal
L14: (375) 13 and logic
L15: (12) 14 and symetrical
L16: (371) 14 and well
L17: (186) 16 and die
L18: (11) "5146117"
Failed
(27) (((semiconductor and gate) and isotropic) and (i

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